N66-26758

Second Quarterly Report

for the

Design and Development of a Non-Dissipative Charge Controller using a Rotary Transformer

Contract No. NAS5-9204

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for

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1. SUMMARY. - This report covers the work accomplished during the second reporting period, and the work to be undertaken during the third period of contract NAS5-9204.

During the second quarter, progress on the rotary transformer was less than desired due to problems in obtaining the necessary ferrite pieces for the transformer core. Near the end of the quarter, however, a prototype rotary transformer was assembled and partially tested. Work was also initiated on the design of an improved transformer.

On the maximum power controller, parts of the system have been breadboarded and partially tested, including a pulse width multiplier and an AC current sample circuit. Limited testing on these circuits was also accomplished. The problem of synchronous rectification of the output of the rotary transformer was also studied during this period. The result of this study (discussed in this report) indicates that synchronous rectification may be ruled out due to the lack of a suitable semiconductor switch.

A simpler technique of maximum power sensing was also studied during this period. This system will eliminate the need for a multiplier, thereby reducing the number of components in the system by 20% to 25%. Further component reduction and simplification may be obtained, since the envisioned system will operate with the same accuracy with reduced circuit tolerances. As a result of the above, it is felt that an extension of the contract may be desirable in order to do a thorough investigation of this new system. Additional time may also be needed on the development of a better rotary transformer, and to perform a more complete testing program on the system.

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5. INTRODUCTION. - The scope of the original contract included means for efficiently converting the available power from irradiated solar panels to levels suitable for charging secondary batteries and for operating electronic equipment. This was to incorporate a rotary transformer to couple the steerable panels to the satellite body reference. It was also intended that high efficiency or so-called "dissipationless" converter principles be incorporated.

Basic in this system are two elements:

1. The transformer itself with the associated inverter circuits;
2. The maximum power controller.

The latter includes a multiplier, synchronous detector, jitter generator, current sample circuit, and a pulse width controller.

During this period, a prototype rotary transformer was completed and partially tested. The design of a more refined rotary transformer was undertaken. Investigation of the optimum configuration for the main converter to drive the rotary transformer with the specific aim of determining the relative merits of the 2-transistor center tap transformer converter as opposed to the 4-transistor single primary winding transformer was also undertaken.

On the maximum power controller, parts of the system were breadboarded and partially tested. These parts included a pulse width multiplier and a current sample circuit.

A study of a simpler method of maximum power controlling was also initiated.

6. DISCUSSION. -

6.1 SYSTEM. - As shown in the attached block diagram, Figure 1, the regulator system consists of the following major components: the main converter with its associated driving oscillator; a rotary transformer; rectifying and filtering circuitry; the main switching regulator; a multiplier circuit used for making the actual power measurements; a jitter generator; a synchronous detector; and, the current transformer used to sample the output current of the rotary transformer.

Briefly, the operation of the system is as follows: The DC voltage from the solar cell is converted to an AC square wave with a frequency somewhat higher than 10kc. The square wave is coupled through the rotary transformer, is rectified and filtered, and is fed to the input of the main duty cycle modulated switching regulator. The current in the secondary of the rotary transformer is full wave sampled by means of a current transformer whose output is rectified and used as a sample of the main line current. This current sample, along with the voltage output of the main rectifier filter, is fed to the input of the multiplier circuit consisting of a duty cycle modulator and an averaging filter.

The output of the multiplier circuit is AC coupled to the input of an AC amplifier and synchronous detector, where it is synchronously detected with an output from the jitter generator circuit as a reference. Jitter is provided by injecting a jitter signal into the control circuit of the main switching regulator. The output of the synchronous detector is fed to the control input of the main pulse width controller. This signal drives the main pulse width controller towards a null in the synchronous detector output. This point is coincident with the maximum power output.

6.2 CIRCUIT DISCUSSION. - The individual portions of the regulating system will be discussed in some detail in order to define their operating requirements and the specific techniques for meeting these requirements.

6.2.1 ROTARY TRANSFORMER. - At the beginning of this work interval, the fabrication of the ferrite cores and shells for the test transformer, see Figure 2, was subcontracted to the Stackpole Carbon Company, of St. Marys, Pennsylvania. Delivery was scheduled to permit the assembly of the transformer in time to make some significant tests. When the time approached, it was discovered that some other work had taken priority and that this contract had been delayed so that it was expedient to change plans. Matrix had on hand from a previous order some small pieces of ferrite from which a preliminary transformer could be made. Plans were therefore made to have them machined locally and then assembled for test. The cementing of the many pieces together not only consumed time, since curing time had to be allowed between each application, but also resulted in a structure having many residual air gaps in series. This, of course, required additional excitation ampere-turns.

6.2.2 MAIN CONVERTER. - The exact configuration for the main converter has not been finalized at this date. Several factors affect the final choice, not the least of which is the modified rotary transformer design. The present feeling is that in order to minimize the wire required in the windings of the rotary transformer, and to allow safe operation at a relatively high voltage level of 40V to 50V, that the bridge configuration will be the ultimate choice.

Certain problems are inherent in this device. Specifically, the problem of guaranteeing that the two transistors on one side of the bridge to not wind up both "on" at the same time for any period of time, since currents drawn under this condition can be rather large. In line with this, the technique of deriving the drive for the switching transistors from what amounts to a current transformer in series with the rotary power transformer is being investigated. This has a two-fold advantage, in that the drive for the switching transistors remains a reasonably fixed proportion of the current drawn through the collector circuit. This results in maximizing the efficiency of the converter from the standpoint of drive, and it has a secondary advantage of not providing the heavy drive at the moment when the main current path might be through two switches on one side of the bridge. A bridge configuration, in addition to reducing the amount of wire required for the main transformer, does provide for considerably better damping of the transformer itself, which is of value in reducing the amount of overshoot spikes on the converter wave form. The problem of overshoot and ringing on the particular type transformer involved is somewhat more severe than in the very tightly coupled torroidal configuration, in that there is an inherent air gap in the transformer which does lead to some leakage flux.

A breadboard converter section was constructed for use in testing the first model of the rotary power transformer. The circuit is of the 2-transistor type designed to drive a push-pull center tapped primary transformer. The circuit of the converter shown in Figure 3 consists of 3 main parts. These are a simple dissipative regulator to provide a regulated voltage for the timing oscillator, the timing oscillator itself, and the main converter consisting of a pair of driven switches and the necessary transients suppressing the drive adjusting components.

The operation of the circuit is as follows: Transistors Q1, Q2, and the zener diode CR1 comprise a simple dissipative regulator to provide a relatively fixed voltage to the input of the timing oscillator. This is necessary to keep the frequency of the timing oscillator constant with the wide fluctuations of the input line from the

solar cells. The timing oscillator consists of a resistively coupled magnetic oscillator consisting of Q3 and Q4, and associated components. This oscillator runs at a frequency slightly higher than 10kc and provides the necessary drive for the main converter switches Q5 and Q6. The use of resistor coupling in this case was to facilitate synchronizing of the magnetic oscillator by means of external signals in order to investigate the effect of frequency on the efficiency of the converter system. Its free-running frequency was chosen at the lower end of the possible operating frequency range in order that it might be synchronized to higher frequencies for testing.

The main converter consists of two power transistors, Q5, and Q6, which function as driven switches, taking their drive from the magnetic oscillator transformer secondary, and converting the DC input from the solar panel to a square wave at the oscillator frequency. Diodes CR4 and CR5 provide reverse transient voltage protection for the converter transistors. The network, consisting of CR5, CR7, zener diode, resistor capacitor combination is used to suppress transient overshoots to the collector of converter transistors Q5 and Q6. These transients are rectified by diodes CR6 and CR7, and when their value exceeds the breakdown of the zener diode which is chosen to be equal to the highest input voltage expected from the solar cells plus a small safety margin. Current is drawn through the zener diode resistor combination back to the main DC bus line. This provides some damping of the overshoot wave form and has the added advantage that it returns some power to the bus line where it can be used.

The converter was connected to the input of the rotary power transformer. The output of the rotary transformer was full wave rectified, filtered, and applied to a load consisting of ordinary incandescent light bulbs for convenience. The number and type of light bulbs was varied in order to vary the power drain on the converter. Initial testing of the converter, rotary power transformer combination, indicated that the concern previously expressed over the increased magnetizing current and leakage reactance produced by multiple air gaps in the transformer core built up of multiple sections was justified. Overshoot transients of a relatively high magnitude and duration were present on the collectors of the converter transistors and the suppression circuit previously discussed was added to suppress these to allow meaningful measurements to be taken. The drive for the final switches was optimized at a power level of approximately 50 watts, and measurements were taken over an input power range of from approximately 28 watts to 80 watts. With

input currents ranging from 1.9 to 3.2 amps, and the voltages of 15V to 25V, the relatively low voltage range was chosen in order to minimize the amount of power lost in the overshoot suppression circuit in order to give a more realistic impression of the actual performance of the converter.

It should be pointed out that the efficiency of the converter at the lower voltages is somewhat less than that which can be obtained in higher voltage levels with an optimized transformer design. This data is shown in the accompanying table (Table 1) and plotted in the accompanying graph (Figure 4). For these tests, the oscillator circuitry was energized separately and the figures represent the performance of the combination of the main converter switches and the rotary power transformer, plus the rectifying diodes. Efficiencies of this combination vary from approximately 81% to a high of somewhat over 88% with the higher efficiencies occurring at the highest voltage level tested, and decrease somewhat with increasing current levels. It is felt at this time that prior to more detailed testing of the 2-transistor converter, that work should proceed with a 4-transistor bridge type converter in order to allow a preliminary evaluation of its performance with the present transformer to be studied and evaluated against the performance of the 2-transistor circuit in order to give a better insight as to which direction the second model of the rotary power transformer design should take. This course is presently being pursued and the bridge type converter circuit will be evaluated during the next reporting period.

As previously stated, work on the second model of the rotary power transformer is in process, and as soon as preliminary testing of the bridge configuration converter is complete, the winding configuration for this model will be chosen and fabrication of the second model of the rotary power transformer will be completed. Preliminary testing to date indicates that the overall efficiency of 85% can reasonably be expected. It is expected that significant improvements in the transformer and the converter itself can be made.

6.2.3 RECTIFYING AND FILTERING CIRCUITRY. - At present, rectification of the output of the rotary transformer is being accomplished by the use of diodes. After being rectified and filtered, the output of the rotary transformer is then again chopped by the pulse width switch of the main switching regulator. The possibility of combining the functions of rectification and pulse width switching into one operation can be seen to hold possible advantages insofar as greater efficiency due to the removal of a voltage drop and greater reliability due to a reduction in the number of components. After study, however, one finds that in this application the only semiconductor devices that are designed for this sort of application are SCR's.

The semiconductor device required must be capable of handling a minimum forward current of 5 amps and be capable of blocking at least 50V in the reverse direction. A preferred device would be capable of handling a minimum of 5 amps in the forward direction and be capable of blocking 50V in the forward direction, and 100V in the reverse direction. The lesser requirements are produced by a circuit which uses two chokes and two recirculating diodes, requiring that the switching device block only in the reverse direction. This system, however, requires the use of much larger chokes, since the choke must supply energy for greater than one-half cycle, and also more current flows through the recirculating diodes which results in higher losses.

The design of transistors is such that they do not readily lend themselves to this type of function, being designed to conduct and block in the same direction. In the reverse direction, a transistor must block with the base-to-emitter diode which normally has a 5V to 15V breakdown rating. If the circuit utilizing two chokes and recirculating diodes is used, there is no necessity of blocking in the forward direction, so that if the transistor is used in the inverted mode (swapping emitter and collector functions), the reverse blocking can be accomplished. The problem with this configuration is that the beta in the inverted mode is less than one at high currents (greater than 1 amp). The drive required, therefore, makes transistors used in this configuration more lossy than diodes.

One device that will meet the breakdown and conduction requirements is a silicon controlled rectifier. The disadvantages of this device are:

(1) It has a high forward drop, since it has a diode in the forward path;
(2) It is slower than a fast switching transistor; and
(3) It requires a more complex driving circuit.

It appears from the above discussion that at the present time, the best technique is the use of diode rectifiers followed by a transistor pulse width switch. Further study, however, will be given to the other techniques.

6.2.4 CURRENT SAMPLE. - The current sample circuit is given in Figure 5. It consists of a current transformer (T2), which samples current in both windings of the rotary transformer secondary. The output of the current transformer is peak-to-peak rectified by a voltage doubler circuit. The load resistor (R1) on the voltage doubler converts the current to a proportional voltage (E1). At low voltages, the non-linearity introduced by the diodes in the doubler introduce a small non-linearity in the current to voltage conversion. As the output voltage increases, the effect of this non-linearity is reduced. The data in Table 2, which is plotted in Figure 6, is a plot of the input current vs the output voltage of the circuit. Figure 5 shows the test configuration from which the data was taken. The current to voltage conversion ratio can be changed by simply changing the load resistance (R1) on the doubler. Curves are plotted for a 1KΩ and a 2KΩ load resistor.

6.2.5 MULTIPLIER. - The multiplier circuit functions as the instantaneous power measuring portion of the regulating system. It accomplishes this by producing a continuous product of the voltage on the main bus and the current drawn through the main bus. This product term is then proportional to the power being drawn from the bus. For the specific use intended here, the absolute value of the power being measured is of little significance, and the desired output is actually the variation of this power level as the effective load is jittered by some small increment. This allows scale factors to be chosen for convenience, and tends to minimize the effects of nonlinearities occuring outside the range of interest.

The multiplier consists basically of a duty cycle modulator, a switch, and an averaging filter. Multiplication occurs in the following fashion: If a voltage is applied to the input of the switch and the duty cycle, or ratio of "on" and "off" times of the switch is varied, it can be seen by inspection or shown by Fourier analysis of the resultant waveform that the average output of the switch is the input voltage times the duty cycle. Consequently, if this average output is then detected by means of an averaging filter, the output of the filter will be a product of the input voltage and the duty cycle. If in turn the duty cycle is made proportional to some other parameter, in this case specifically the bus line current, the result is the product of the bus line current and voltage, which of course is power. This assumes only that the rates of variations in the two parameters being multiplied are sufficiently slower than the switching rate of the duty cycle modulator such that the output can be properly filtered without attenuating the variations caused by either input.

Detailed operation of the circuit (Figure 7) is as follows: Transistors Q2 and Q3 form a differential pair which functions as a voltage comparator. The emitters of Q2 and Q3 are fed by a constant current source comprised of transistor Q4 and associated resistors. The purpose of the constant current source is to hold the operating point of the differential stage constant with relatively wide swings at the two inputs and to provide maximum coupling between the two halves of the differential amplifier. The base of Q2 is driven with a linear ramp generated by constant current generator Q1 and associated resistors, which charges capacitor C1 at a linear rate. The ramp is reset to ground once per cycle of the main oscillator by shunt switch Q8 which is driven by a differentiated output from the oscillator. The output of the current sample circuit is fed to the

other input of the voltage comparator which is the base of Q3.

If the action of the circuit is considered from the time the ramp has been reset, it may be seen that Q3 at this time is conducting, which in turn causes Q7 to be in the "on" or conducting state through the action of the driver transistors Q5 and Q6. Excessive gain is used between the output of the comparator and the switch transistor Q7 in order to sharpen the switching time. As the ramp rises, it ultimately reaches an amplitude where it equals or slightly exceeds the voltage at the base of Q3 and causes the differential amplifier to swing in the opposite direction, i.e., Q2 conducting and Q3 heading toward cut-off.

When this condition occurs, Q7 will go to the "off" state, again through the action of driver transistors Q5 and Q6. When Q7 is in the "off" state, the clamping diodes, CR1 and CR2, in conjunction with the current source Q8, hold the output of Q7 at ground level. If the ramp is linear, the time required to reach this state is a function of the voltage at the base of Q3, which is in turn a function of the current through the main bus. As this level is raised and lowered, the duty cycle of the series switch Q7 is raised and lowered in direct proportion to the control signal. The output of Q7 is averaged by means of a multisection RC filter in order to obtain the average value which then yields the desired product term.

Test results on the multiplier are tabulated in Table 3, and plotted in Figure 8. E_S was held constant while E_1 was varied through its operating range. This was then repeated for various levels of E_S. For a given E_S value, the output of the multiplier should be a linear function of E_1. This is demonstrated in Figure 8. It can be seen, however, that there appears to be a small offset in the output. This is caused by missmatch in the differential amplifier, storage time in the series switch transistor Q7, and the finite rise and fall times of the output of Q7. In operation, however, the multiplier is never required to operate at less than a 20% duty cycle, so that the nonlinearity at low levels causes no problems.

An obvious alternative approach to the duty cycle modulation portion of both the multiplier and the main power controller would be the use of a magnetic amplifier as the current or voltage-to-duty cycle converters. A cursory examination of the alternatives would

seem to indicate that although the magnetic amplifier has certain advantages, specifically in that its control winding may be placed directly in a DC line thus making it quite convenient from the standpoint of sampling DC current. It does suffer from certain disadvantages which tend to reduce the desirability of this approach. The magnetic amplifier is basically a non-linear device requiring use of fairly extensive feedback to linearize it to the point where a multiplier output would be a reasonable function of the true output power. A fair amount of additional circuitry is necessary to obtain reasonably fast switching waveforms from the device without the need for throwing away a lot of power. It is relatively inflexible in that any type of scale change is effected by redesigning and rewinding the device. It is somewhat expensive to build in the special configurations required for this case. It also has a rather slow speed of response if one attempts to de rive much gain from it, which while not particularly important for this specific usage, would tend to narrow the range of possible applications for the multiplier device.

Further comparisons between the two techniques, namely that of circuit techniques as opposed to magnetic amplifier techniques for the duty cycle conversion, will be carried out to insure that the technique which has been chosen for the moment is at least as good as the magnetic amplifier approach.

6.2.6 SYNCHRONOUS DETECTOR. - The function of the synchronous detector (Figure 9) is to provide a DC output which is a function of both the phase and amplitude of the jitter frequency output of the multiplier. To accomplish this, the jitter frequency output of the multiplier is AC amplified and synchronously detected by means of a shunt chopper which takes its drive from the jitter generator. This drive signal is phase shifted somewhat to compensate for the phase shift in the input signal to the detector, due to filtering of the main bus line and the response of the main pulse width regulator.

Following the chopper is a 2-stage DC amplifier which boosts the signal level and in addition performs the final rectification. Although both a positive and negative output would be available from this circuit, the positive output only is taken since the single sided output is sufficient to control the main pulse width converter. The control circuit operation is such that the output of the synchronous detector is essentially zero up to the point of maximum power, and then rises in a positively-going direction very sharply as the maximum power point is reached. This rise is commensurate with the phase reversal which occurs at the multiplier output at the point where maximum power is reached. This output is then fed to the main pulse width converter and used to control the duty cycle of the main regulator in such a manner as to hold the power drawn from the main bus at a point very near the maximum power level.

6.2.7 MAIN PULSE WIDTH CONTROLLER. - The main pulse width controller (Figure 10) again consists of a duty cycle modulator and series switch and functions in a very similar fashion to the duty cycle modulator used for the multiplier circuit, with the exception that in this case, the duty cycle is made proportional to the output from the synchronous detector. In this circuit, as in the multiplier, the control signal from the synchronous detector is compared with a linear ramp by means of a differential comparator which controls the series switch through its associated driver transistor stages in such a manner as to vary its duty cycle as a function of the input signal from the synchronous detector.

The sense of this circuit is opposite to that of the multiplier in that an increasing input from the synchronous detector yields a longer "off" time and consequently a lower duty cycle. In addition, the ramp in this case is reset once per half cycle of the timing oscillator, and the jitter is injected into this control by means of a transistor switch which switches the resistor in and out of the divider for the current source, thus producing a modulation of the current source output and a variation slope of the ramp generated by the current source and its capacitor. This, of course, modulates the duty cycle of the main controller switch and acts as a varying load on the output of the rotary transformer. The main power input to the controller is taken directly from the rectified output of the main rotary transformer. The output of the switch is averaged by means of an LC filter which uses a recycle diode in order to provide a path for the current flow which occurs when the stored energy in the inductor is released into the load during the "off" portion of the cycle. The output of the main controller is then fed to the load which consists of the battery and the rest of the output load.

6.2.8 JITTER GENERATOR. - The jitter generator is simply a low frequency oscillator running at approximately 10 cycles per second which provides the drive for the synchronous detector and the switch which introduces the jitter into the main switching regulator.

6.3 SIMPLIFIED MAXIMUM POWER CONTROLLER. - During the second reporting period a technique resulting in a simpler method of maximum power controlling was studied. In the original system, the operating power level is found by multiplying the current by the voltage at some point in the circuit. In order to construct a circuit that will accurately find the maximum power point, a linear current sample circuit and a linear multiplier circuit are necessary.

If the load that is being driven has an always increasing power vs load current curve, then maximum power can be sensed as maximum load current. The advantages to this type of a system are: (a) there is a reduction in the number of components, since a multiplier is not necessary, and (b) the current sample circuit is not required to be linear, it must only increase in output voltage for an increase in current.

The reliability of this type of a system is higher, due to both a reduction in the number of components and the reduction in the stability required of others. Figure 11 is a block diagram of this system. It is noticed that most of the blocks have already been developed in the original system, allowing the technique to be tried with a minimum of development. The one part of the system which is not developed is the current sample circuit. This could possibly be as simple as a current transformer, since only the variations of the load current are desired, the absolute level being unimportant. The operation of the control loop is similar to the original system, with the exception that the load current is maximized instead of the output of the multiplier.

7. NEW TECHNOLOGY. - During this reporting interval, there were no technologies developed which would fall under this category.

8. PROGRAM FOR NEXT REPORTING INTERVAL. - During the next quarter, it is planned to have working a maximum power controller which is operating in conjunction with the rotary transformer. This system will make use of a pulse width modulated multiplier to measure the power. It is also expected that a system which maximizes the power by maximizing the current into the load will be breadboarded. The work planned on each piece of the system is discussed below.

Rotary Transformer. Testing of the prototype rotary transformer will continue and the fabrication of the final unit will be started and will be completed near the end of the next period or early in the following period.

Main Converter. More work will be done on determining the optimum drive configuration for the main converter. Some of this work, however, will have to be delayed until the completion of the final rotary transformer.

Maximum Power Controller. The remaining parts of the maximum power controller will be breadboarded and the entire system tested.

Work will also be started on simulated solar panel and load resistances. Since both the source resistance (solar cell resistance) and the load resistance (batteries and pulse width regulator) are very non-linear, it is considered important to build simulators for the source and load resistances in order to properly test the system.

9. CONCLUSIONS AND RECOMMENDATIONS. - From the results that have been obtained to this date, there appears to be no major obstacle to meeting the technical requirements of the contract. However, in order to produce the optimum system, we feel that additional time will probably be required.

This time would be spent primarily in three areas: (1) redesigning the rotary transformer to produce a lighter and more efficient unit, (2) studying and implementing the simplified method of maximum power controlling described in the discussion, and (3) designing and building source and load simulators and using these to perform more detailed testing of the overall system.

APPLICATION			REVISIONS			
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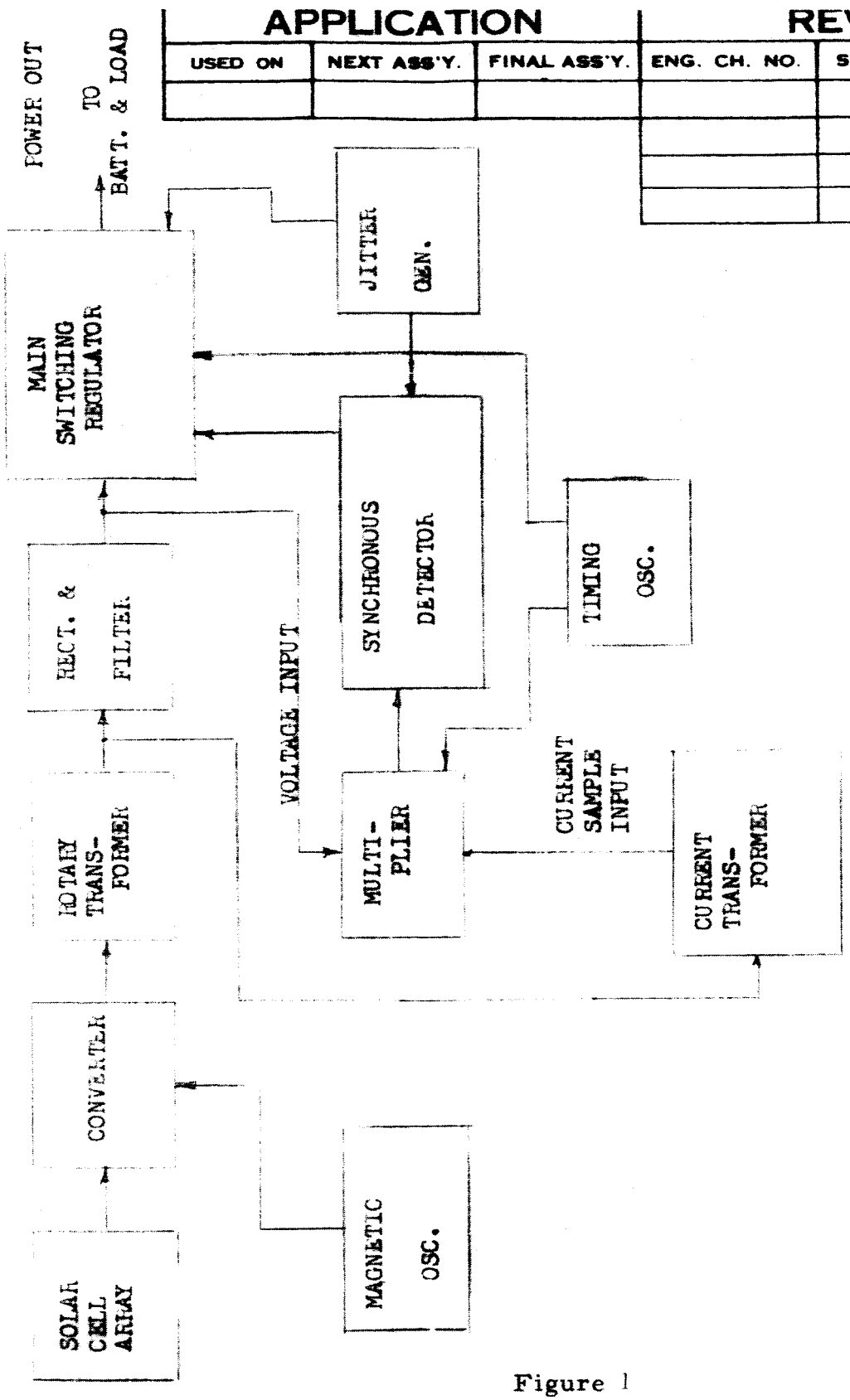

Figure 1

UNLESS OTHERWISE NOTED	DR.	DATE
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DEBURR	MFG. APPD	
MAT'L:		

Matrix RESEARCH AND DEVELOPMENT CORP.
NASHUA, NEW HAMPSHIRE

TITLE BLOCK DIAGRAM
NON-DISSIPATIVE CHARGE CONTROLLER

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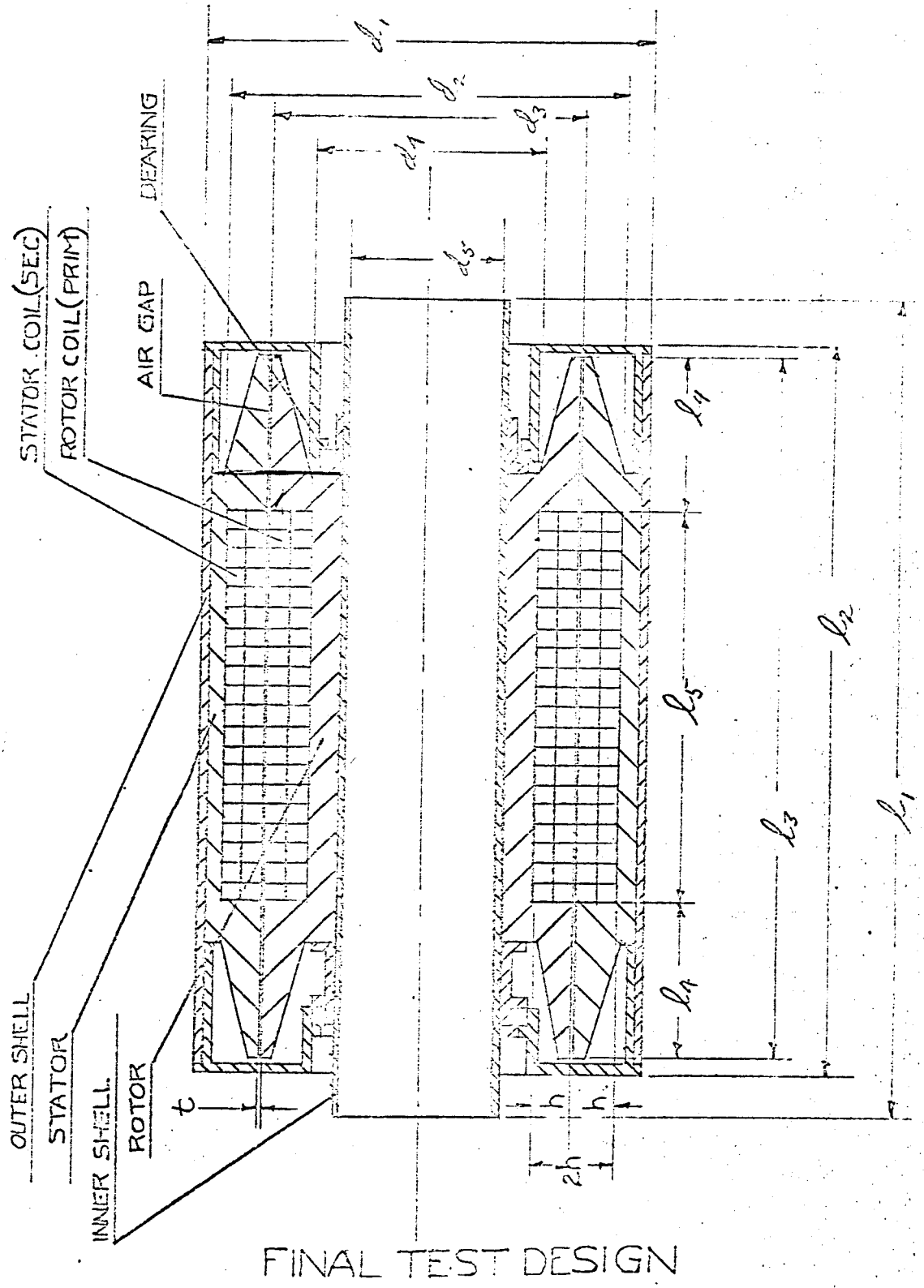
BEARING
AIR GAP
STATOR COIL (SEC.)
ROTOR COIL (PRIM.)
OUTER SHELL
STATOR
INNER SHELL
ROTOR
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h
h
2h
FINAL TEST DESIGN

Figure 2

APPLICATION			REVISIONS			
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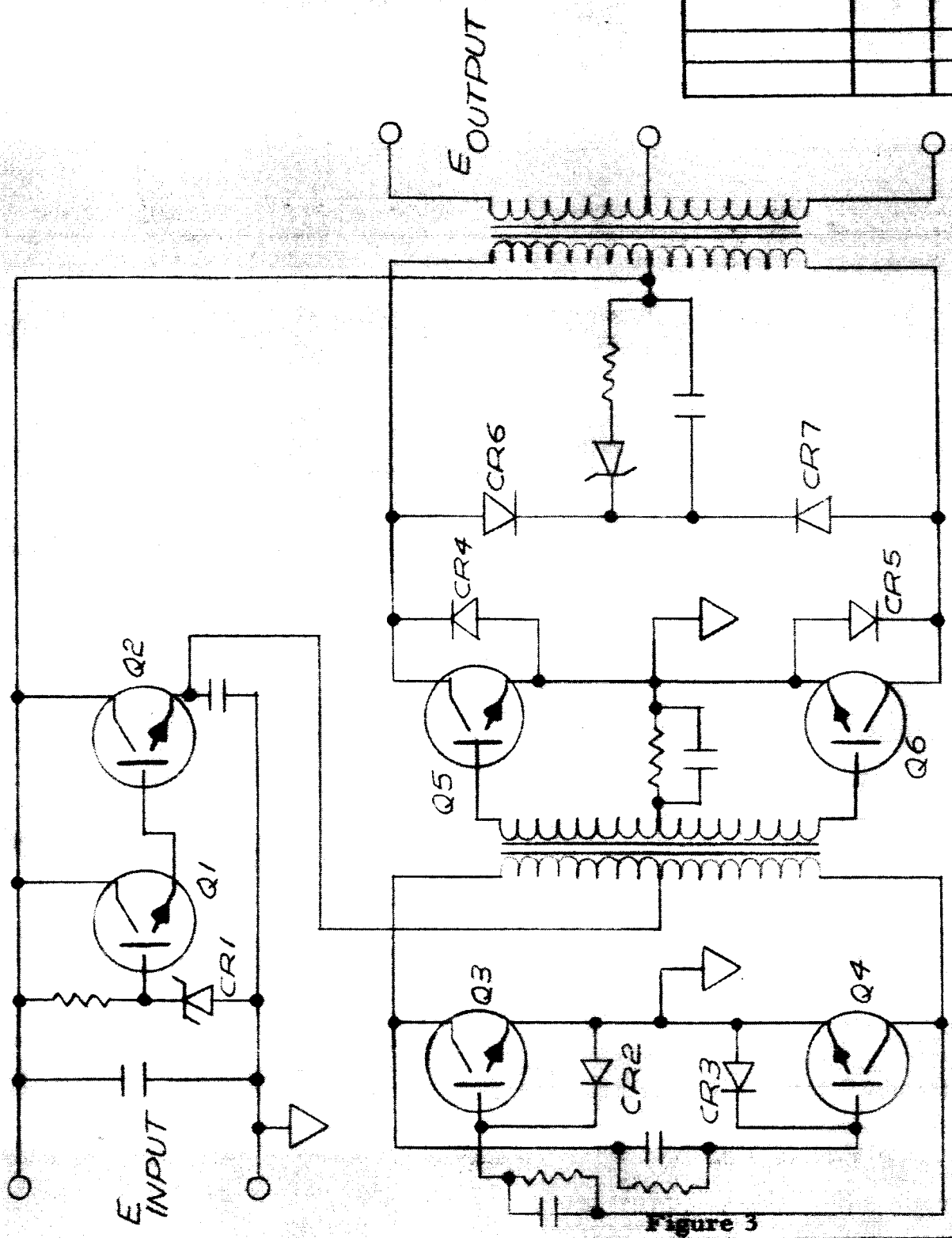

Figure 3

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	CHK.	
	ENG. APPD	
	MFG. APPD	
MAT'L:		

Matrix RESEARCH AND DEVELOPMENT CORP.
NASHUA, NEW HAMPSHIRE

TITLE
MAIN CONVERTER

SCALE	SIZE	
	A—	
	CODE	OF

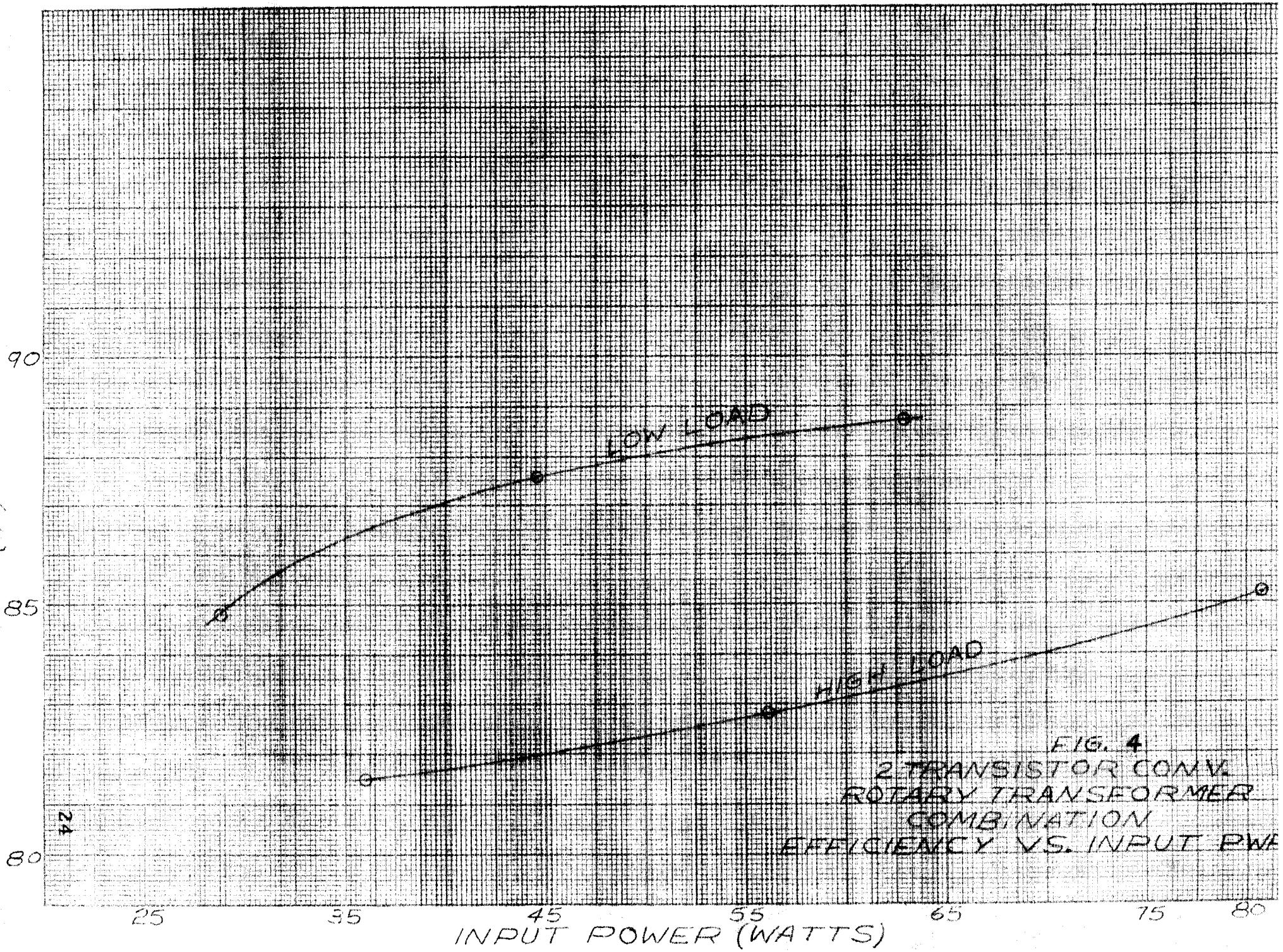

FIG. 4
2 TRANSISTOR CONV.
ROTARY TRANSFORMER
COMBINATION
EFFICIENCY VS. INPUT PWR

APPLICATION			REVISIONS			
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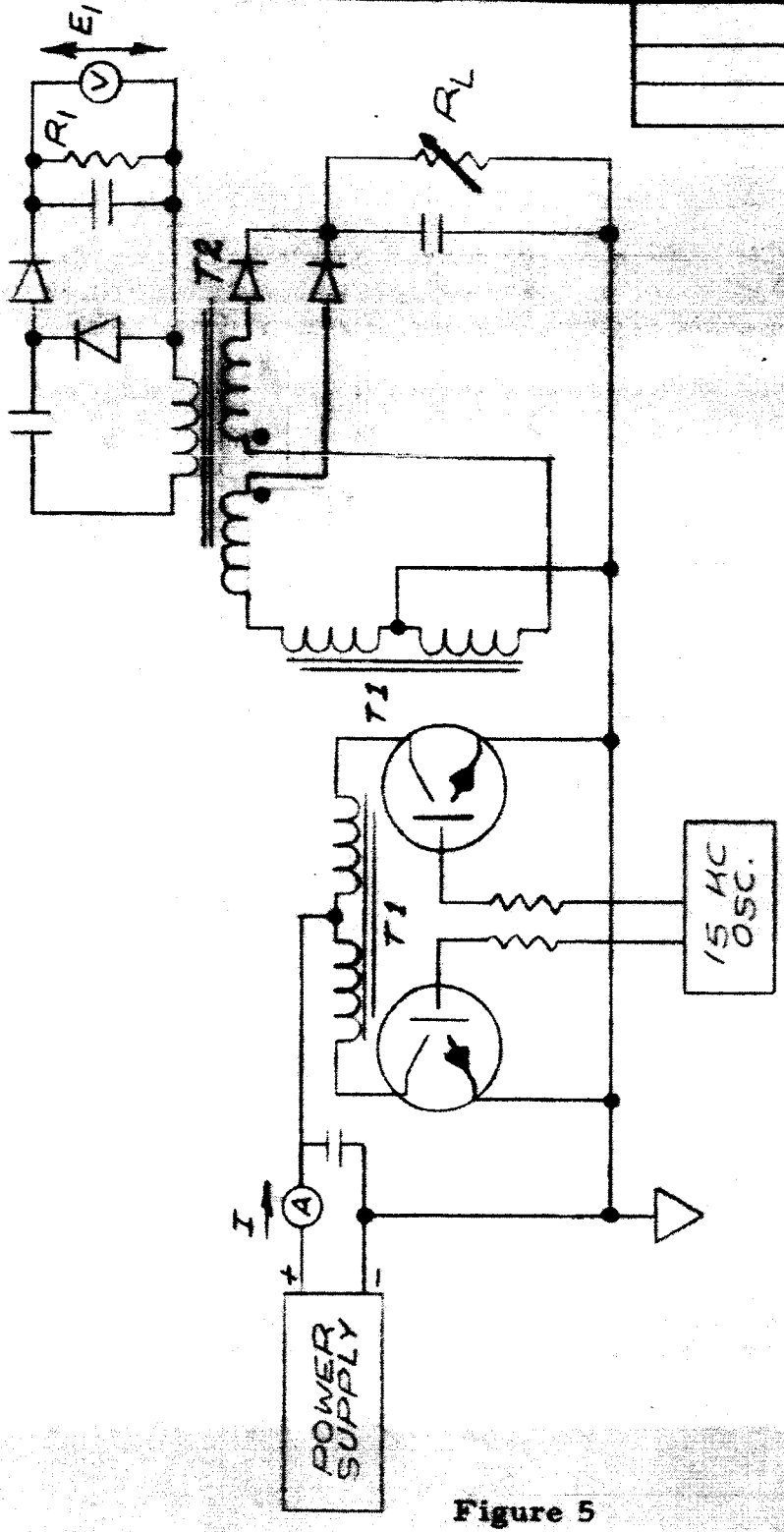

Figure 5

UNLESS OTHERWISE NOTED	DR.	DATE
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DEBURR	MFG. APPD	
MAT'L:		

Melpix RESEARCH AND DEVELOPMENT CORP.
NASHUA, NEW HAMPSHIRE

TITLE CURRENT SAMPLE CKT. AND TEST SET UP

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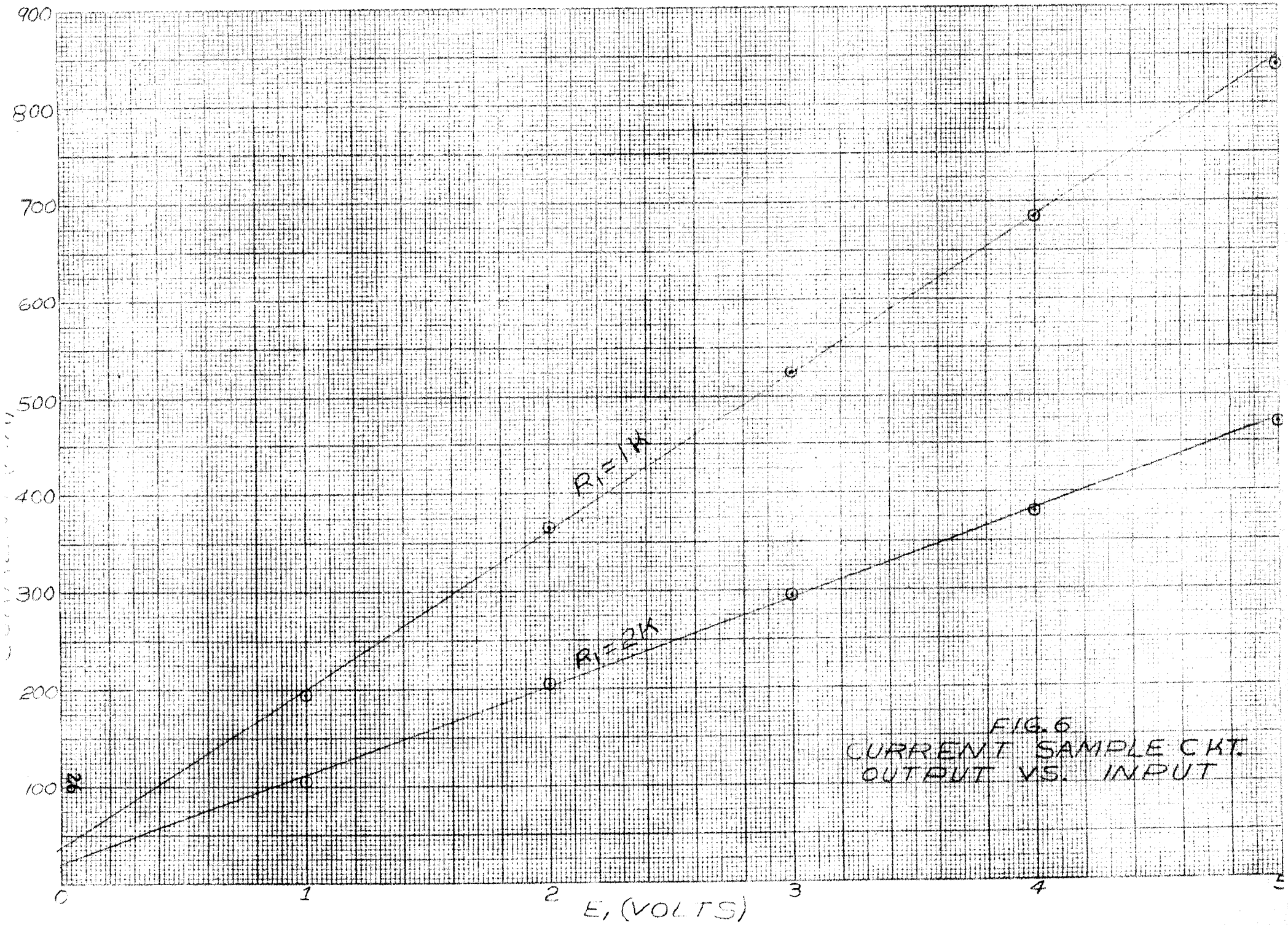

FIG. 6
CURRENT SAMPLE CKT.
OUTPUT VS. INPUT

APPLICATION			REVISIONS			
USED ON	NEXT ASS'Y.	FINAL ASS'Y.	ENG. CH. NO.	SYM	DATE	APPROVED

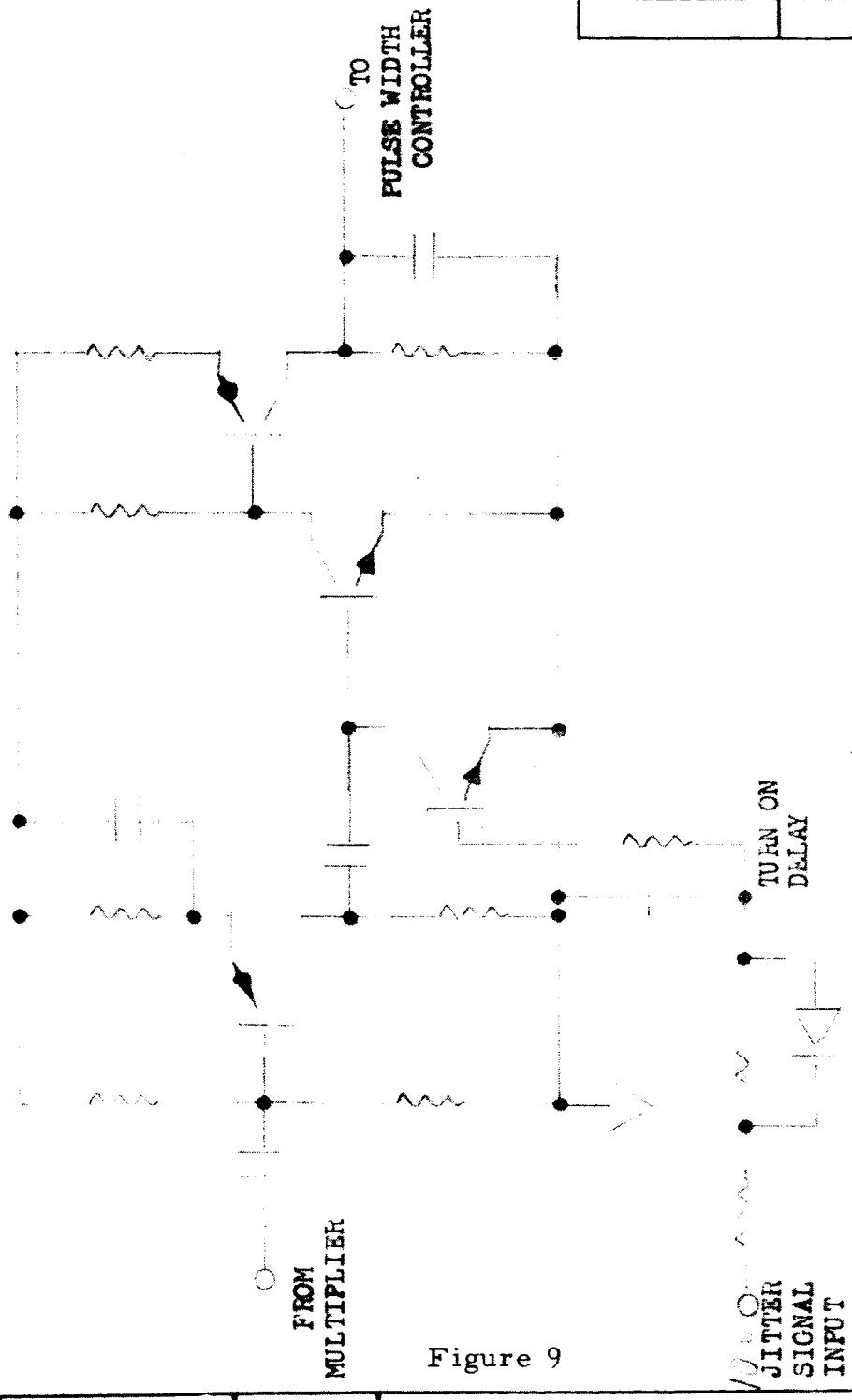

Figure 9

UNLESS OTHERWISE NOTED	DR.	DATE	Matrix RESEARCH AND DEVELOPMENT CORP. NASHUA, NEW HAMPSHIRE
DIMENSIONS ARE IN INCHES	CHK.		
TOLERANCES DEC. ± .005 FRAC. ± 1/64 ANGLES ± 1/4°	ENG. APPD		TITLE SCHEMATIC SYNCHRONOUS DETECTOR
DEBURR	MFG. APPD		
MAT'L:			SCALE / DWG. NO. A—
			CODE / OF

APPLICATION			REVISIONS			
USED ON	NEXT ASS'Y.	FINAL ASS'Y.	ENG. CH. NO.	SYM	DATE	APPROVED

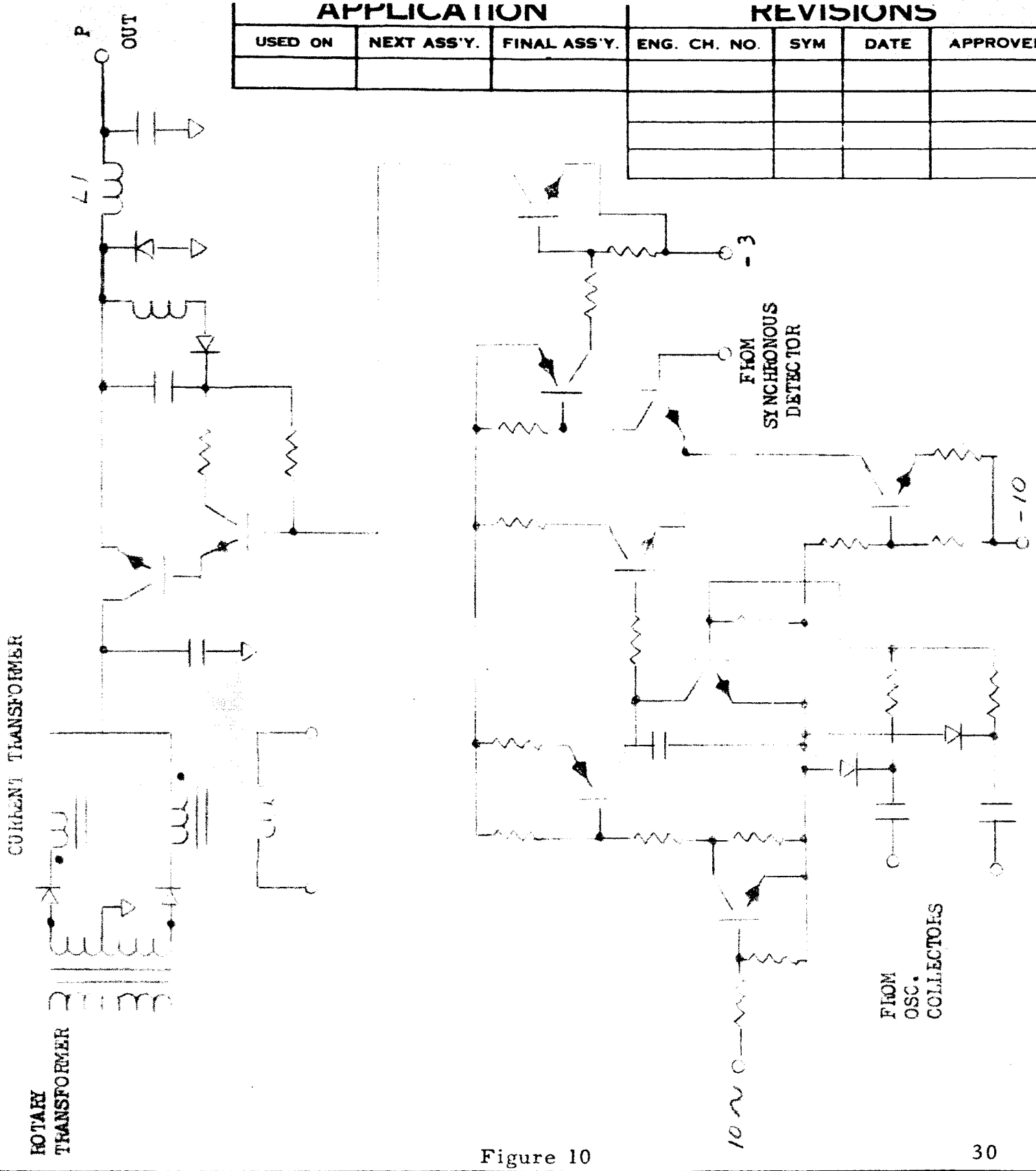

Figure 10

UNLESS OTHERWISE NOTED	DR.	DATE
DIMENSIONS ARE IN INCHES	CHK.	
TOLERANCES DEC. ± .005 FRAC. ± 1/64 ANGLES ± 1/4°	ENG. APPD	
DEBURR	MFG. APPD	
MAT'L:		

Matrix RESEARCH AND DEVELOPMENT CORP.
NASHUA, NEW HAMPSHIRE

TITLE SHCEMATIC
P.W. CONTROLLER

SCALE	DWG. NO. A—	
	CODE	OF

APPLICATION			REVISIONS			
USED ON	NEXT ASS'Y.	FINAL ASS'Y.	ENG. CH. NO.	SYM	DATE	APPROVED

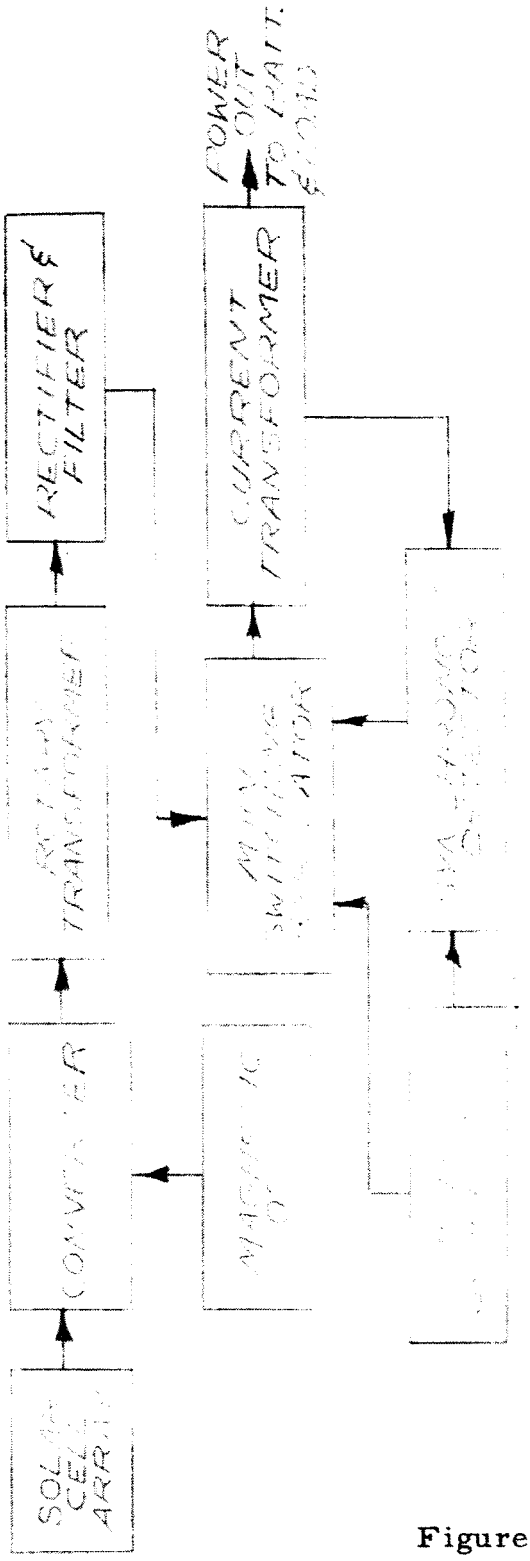

Figure 11

UNLESS OTHERWISE NOTED	DR. J. SLU	DATE 3-15-66	Matrix RESEARCH AND DEVELOPMENT CORP. NASHUA, NEW HAMPSHIRE
DIMENSIONS ARE IN INCHES	CHK.		
TOLERANCES DEC. ± .005 FRAC. ± 1/64 ANGLES ± 1/4°	ENG. APPD		TITLE
DEBURR	MFG. APPD		
MAT'L:			SCALE / DWG. NO. A— / CODE / OF

APPLICATION			REVISIONS			
USED ON	NEXT ASS'Y.	FINAL ASS'Y.	ENG. CH. NO.	SYM	DATE	APPROVED

Test Data on 2-Transistor Converter and Rotary Transformer

E_{in}	I_{in}	P_{in}	E_o	I_o	P_o	Efficiency
15	1.912	28.68	12.22	1.990	24.32	84.80
20	2.228	44.56	16.83	2.318	39.01	87.54
25	2.518	62.95	21.33	2.618	55.84	88.70
15	2.402	36.03	11.64	2.522	29.36	81.48
20	2.896	56.12	15.82	2.938	46.48	82.82
25	3.230	80.75	20.50	3.356	68.80	85.20

Table 1

UNLESS OTHERWISE NOTED	DR.	DATE	Matrix RESEARCH AND DEVELOPMENT CORP. NASHUA, NEW HAMPSHIRE
DIMENSIONS ARE IN INCHES	CHK.		
TOLERANCES DEC. ± .005 FRAC. ± 1/64 ANGLES ± 1/4°	ENG. APPD		TITLE
DEBURR	MFG. APPD		
MAT'L:			SCALE / DWG. NO. A— / CODE / OF

USED ON	NEXT ASS'Y.	FINAL ASS'Y.	ENG. CH. NO.	SYM	DATE	APPROVED

E_1	I (R_1 = 1K)	I (R_1 = 2K)
1	195 ma	105 ma
2	365 ma	205 ma
3	525 ma	295 ma
4	685 ma	380 ma
5	840 ma	470 ma

Test Data on Current Sample Circuit

Table 2

UNLESS OTHERWISE NOTED	DR.	DATE	Matrix RESEARCH AND DEVELOPMENT CORP. NASHUA, NEW HAMPSHIRE
DIMENSIONS ARE IN INCHES TOLERANCES DEC. ± .005 FRAC. ± 1/64 ANGLES ± 1/4° DEBURR	CHK.		
	ENG. APPD		TITLE
	MFG. APPD		
MAT'L:			SCALE / DWG. NO. A—
			CODE / OF

APPLICATION			REVISIONS			
USED ON	NEXT ASS'Y.	FINAL ASS'Y.	ENG. CH. NO.	SYM	DATE	APPROVED

E_1	E_S = 30V Duty Cycle	E_o	E_S = 20V Duty Cycle	E_o	E_S = 10V Duty Cycle	E_o
.2V	9%	2.44V	8%	1.50V	8%	.59V
.5V	14%	3.98V	13%	2.54V	13%	1.12V
1.0V	23%	6.65V	22%	4.32V	22%	2.02V
1.5V	33%	9.43V	32%	6.18V	32%	2.97V
2.0V	42%	12.26V	42%	8.03V	41%	3.90V
3.0V	62%	17.88V	62%	11.82V	60%	5.80V
4.0V	82%	23.47V	81%	15.61V	80%	7.70V
5.0V	99%	29.13V	98%	19.35V	97%	9.60V

Test Data on Multiplier

Table 3

UNLESS OTHERWISE NOTED	DR.	DATE	Matrix RESEARCH AND DEVELOPMENT CORP. NASHUA, NEW HAMPSHIRE		
DIMENSIONS ARE IN INCHES	CHK.				
TOLERANCES DEC. ± .005 FRAC. ± 1/64 ANGLES ± 1/4°	ENG. APPD		TITLE		
DEBURR	MFG. APPD				
MAT'L:			SCALE	DWG. NO. A—	
				CODE	OF